

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
25 August 2005 (25.08.2005)

PCT

(10) International Publication Number
WO 2005/078790 A1

(51) International Patent Classification⁷: **H01L 21/768**,
23/532, G02F 1/1362

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(21) International Application Number:
PCT/KR2005/000392

(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,
KG, KP, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG,
MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH,
PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(22) International Filing Date: 11 February 2005 (11.02.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10-2004-0008956
11 February 2004 (11.02.2004) KR

(84) Designated States (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO,
SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, ML, MR, NE, SN, TD, TG).

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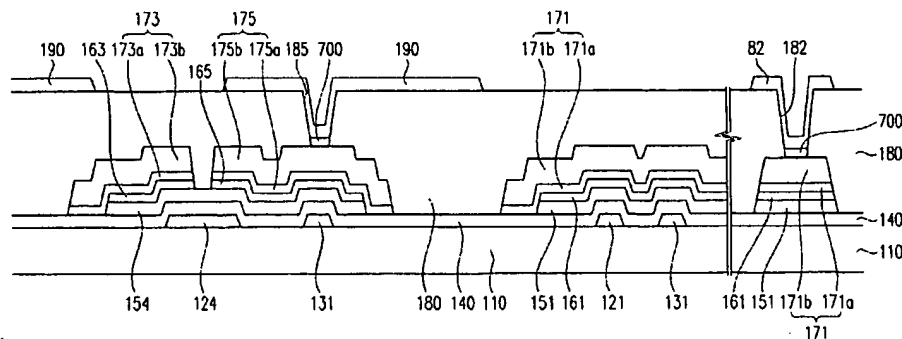
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Published:

- with international search report
- before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments

*For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*

(54) Title: CONTACT PORTION AND MANUFACTURING METHOD THEREOF, THIN FILM TRANSISTOR ARRAY PANEL
AND MANUFACTURING METHOD THEREOF



(57) Abstract: A method of manufacturing a contact portion is provided, which includes: forming a first signal line on a substrate (110), forming an insulating layer (140) covering the first signal line and having a contact hole (182, 185) exposing the first signal line; forming a contact layer (700) on the exposed surface of the first signal through the contact hole; and forming a second signal line (82, 190) connected to the first signal line via the contact layer. Wherein the first signal line is made of Al or Al alloy, and the second signal line is made of ITO or IZO.

WO 2005/078790 A1

Description

CONTACT PORTION AND MANUFACTURING METHOD THEREOF, THIN FILM TRANSISTOR ARRAY PANEL AND MANUFACTURING METHOD THEREOF

Technical Field

- [1] The present invention relates to a contact portion, method for manufacturing the same, a thin film transistor array panel, and a method of fabricating the same.

Background Art

- [2] Thin film transistor array panel is used as a circuit substrate to individually drive each pixel, such as of liquid crystal display or organic electro luminescence display. The thin film transistor array panel includes a plurality of pixels arranged in a matrix and a plurality of signal lines for driving the pixels such as gate lines for transmitting scanning signals and data lines for transmitting data signals. Each pixel includes a pixel electrode, and a thin film transistor (TFT) connected to the gate lines and the data lines for controlling the data signals.
- [3] At this time, signal lines such as gate lines and the data lines includes metal materials, and the pixel electrodes are usually made of transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). ITO or IZO in a liquid crystal display may be used as a contact assistant layer to reinforce contact characteristics when connecting the gate lines and the data lines to external drive circuits.
- [4] In order to prevent delay or distortion of signals, the signal lines are generally made of materials having low resistivity such as aluminum or aluminum alloy. However, since the physical and the chemical properties of the aluminum or aluminum alloy is not good, that is, the aluminum or aluminum alloy is easily oxidized and broken, when connecting other conductive material in a contact portions, accordingly the characteristics of semiconductor devices are deteriorated. Furthermore, in the case that ITO and IZO as a transparent electrode such as in a liquid crystal display is used to reinforce contact portions of aluminum. However, because of the poor contact properties between aluminum or aluminum alloy and ITO, or IZO, a different material such as Ti, Cr, Mo is then inserted therebetween. Accordingly, the manufacturing method is complicated and production costs are increased.
- [5] Furthermore, when removing aluminum in the contact portions to expose a material layer having good contact characteristic, an under-cut structures are frequently generated by over-etching the Al containing metal under a sidewall of the contact portions. The undercut yields disconnection or poor profile of the subsequently-formed layer near the undercut to increase the contact resistance of the contact portions.

Disclosure of Invention

Technical Problem

- [6] It is therefore an object of the present invention to provide contact structures having good contact properties of wiring made a material of low resistivity and methods for manufacturing the same.
- [7] It is another object of the present invention to provide a thin film transistor array panels having contact structures of good contact properties and methods for manufacturing the same.
- [8] It is another object of the present invention to simplify manufacturing methods of thin film transistor array panels for liquid crystal displays.

Technical Solution

- [9] A method of manufacturing a contact portion is provided, which includes: forming a first signal line on a substrate; forming an insulating layer covering the first signal line and having a contact hole exposing the first signal line; forming a contact layer on the exposed surface of the first signal through the contact hole; and forming a second signal line connected to the first signal line via the contact layer. Wherein the first signal line is made of Al or Al alloy, and the second signal line is made of ITO or IZO.
- [10] The substrate may be soaked in chemical conversion solution including a conductive material to form the contact layer.
- [11] The chemical conversion solution may include at least one of W, Zr, Mo, and Cr.
- [12] A method of manufacturing a thin film transistor array panel is provided, which includes: forming a gate line on a substrate; forming a gate insulating layer; forming a semiconductor layer; forming an ohmic contact layer; forming a data line and a drain electrode; forming a passivation layer having a first contact hole exposing the portion of the drain electrode; and forming a first contact layer on the exposed surface of the drain electrode through the first contact hole.
- [13] The substrate may be soaked in chemical conversion solution including a conductive material to form the contact layer.
- [14] The chemical conversion solution may include at least one of W, Zr, Mo, and Cr.
- [15] A second contact hole exposing the end portion of the gate line or the data line may be formed in the step of forming the passivation layer, and a second contact layer may be formed on the exposed surface of the gate line or the data line through the second contact hole in the step of forming the first contact layer.
- [16] The method may further include forming a storage electrode line with the same layer as the gate line.
- [17] The method may further include forming a second contact hole exposing the end portion of the gate line, the data line and the storage electrode line in the step of

forming the passivation layer, and forming a second contact layer on the exposed surface of the gate line, the data line and the storage electrode line through the second contact hole in the step of forming the first contact layer.

- [18] A contact portion comprising is provided, which includes: a substrate; a first signal line formed on a substrate; a insulating layer covering the first signal line and having a contact hole exposing the first signal line; a contact layer on the exposed surface of the first signal through the contact hole; and a second signal line formed on the insulating layer and connected to the first signal line via the contact layer. Wherein the first signal line is made of Al or Al alloy, and the second signal line is made of ITO or IZO.
- [19] The contact layer may include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr.
- [20] The contact portion may further comprise a lower layer formed under the first signal line, and the lower layer is a conductive layer including at least one of Cr, Ti, Mo, and MoW alloy.
- [21] A thin film transistor array panel is provided, which includes: a substrate; a gate line formed on an substrate; a gate insulating layer covering the gate line; a semiconductor layer formed on the gate insulating layer; a data line intersecting the gate line and having a source electrode overlapping the portion of the semiconductor layer; a drain electrode overlapping the portion of the semiconductor layer; a passivation layer covering the data line and the drain electrode, and having a first contact hole exposing the portion of the drain electrode; a first contact layer formed on the exposed surface of the drain electrode through the first contact hole, and made of a conductive oxide layer; and a pixel electrode formed on the passivation layer and connected to the drain electrode via the first contact layer.
- [22] The panel may further comprise a color filter formed on the data line and the drain electrode.
- [23] The panel may further comprise a storage electrode line formed with the same layer as the gate line.
- [24] The storage electrode line may include Al and Al alloy.
- [25] The passivation layer and the gate insulating layer may have a second contact hole exposing the portion of the storage electrode line, the panel may further comprise a second contact layer formed on the exposed portion on the storage electrode line through the contact hole, and a contact assistant connected to the exposed portion of the storage electrode line via the second contact layer.
- [26] The passivation layer and the gate insulating layer may have a second contact hole exposing the portion of the storage electrode line, further comprise a second contact layer formed on the exposed portion on the storage electrode line through the contact hole, and a contact assistant connected to the exposed portion of the storage electrode

line via the second contact layer.

- [27] The panel may further comprise an ohmic contact layer formed between the data line and the drain electrode, and the semiconductor layer, the ohmic contact layer has the same planar shape as the data line and the drain electrode, and the semiconductor layer has the planar shape as the data line and the drain electrode except for the channel portion between the drain electrode and the source electrode.
- [28] The first contact layer may include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr, and the gate line may include a conductive layer made of Al or Al alloy.
- [29] The data line may include a first conductive layer made of Al or Al alloy, and the data line may further comprise a second conductive layer formed under the first conductive layer.
- [30] The second conductive layer is made of a conductive layer including at least one of Cr, Ti, Mo, and MoW alloy.

Advantageous Effects

- [31] In the TFT array panel according to an embodiment of the present invention, the signal lines made of Al or Al alloy with low resistivity are easily applicable by forming the contact layers, such that the TFT array panel with large scale and high fineness is provided.

Brief Description of the Drawings

- [32] The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawings in which:
- [33] Fig. 1 is a layout view of an exemplary TFT array panel for an LCD according to an embodiment of the present invention;
- [34] Fig. 2 is a sectional view of the TFT array panel shown in Fig. 1 taken along the line II-II';
- [35] Figs. 3, 5, 7 and 9 are layout views of the TFT array panel shown in Figs. 1 and 2 in intermediate steps of a manufacturing method thereof according to an embodiment of the present invention;
- [36] Figs. 4, 6, 8 and 10 are sectional views of the TFT array panel shown in Figs. 3, 5, 7 and 9 taken along the lines IIIB-IIIB', IVB-IVB', VB-VB', and VI-VI', respectively;
- [37] Fig. 11 is a sectional view of the TFT array panel following the step shown in Fig. 10;
- [38] Fig. 12 is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention;
- [39] Fig. 13 is sectional view of the TFT array panel shown in Fig. 12 taken along the line IX-IX';

- [40] Figs. 14, 18, and 20 are layout views of the TFT array panel shown in Figs. 12 and 13 in intermediate steps of a manufacturing method thereof according to another embodiment of the present invention;
- [41] Fig. 15 is sectional view of the TFT array panel shown in Fig. 14 taken along the lines XB-XB';
- [42] Fig. 16 is a sectional view of the TFT array panel following the step shown in Fig. 15;
- [43] Fig. 17 is a sectional view of the TFT array panel following the step shown in Fig. 16;
- [44] Fig. 19 is sectional view of the TFT array panel shown in Fig. 18 taken along the lines XIIB-XIIB';
- [45] Fig. 21 is sectional view of the TFT array panel shown in Fig. 20 taken along the lines XIVB-XIVB';
- [46] Fig. 22 is a sectional view of the TFT array panel following the step shown in Fig. 21;
- [47] Fig. 23 is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention;
- [48] Fig. 24 is sectional view of the TFT array panel shown in Fig. 23 taken along the line XVII-XVII';
- [49] Figs. 25 and 27 are layout views of the TFT array panel shown in Figs. 23 and 24 in intermediate steps of a manufacturing method thereof according to another embodiment of the present invention;
- [50] Fig. 26 is sectional view of the TFT array panel shown in Fig. 25 taken along the lines XVIII-XVIII';
- [51] Fig. 28 is sectional view of the TFT array panel shown in Fig. 27 taken along the lines XIX-XIX';
- [52] Fig. 29 is a sectional view of the TFT array panel following the step shown in Fig. 28.

[53] DESCRIPTION OF THE REFERENCE NUMERALS IN THE DRAWINGS

- [54] 110: insulating substrate
- [55] 121: gate line
- [56] 124: gate electrode
- [57] 131: storage electrode line
- [58] 140: gate insulating layer
- [59] 151, 154: semiconductor layer
- [60] 161, 163, 165: ohmic contact layer
- [61] 171: data line
- [62] 173: source electrode

- [63] 175: drain electrode
- [64] 700: contact layer
- [65] 180: passivation layer
- [66] 181, 182, 185: contact hole
- [67] 190: pixel electrode
- [68] 81, 82: contact assistant

Best Mode for Carrying Out the Invention

- [69] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.
- [70] In the drawings, the thickness of layers, films and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.
- [71] Now, TFT array panels and manufacturing methods thereof according to embodiments of the present invention will be described with reference to the accompanying drawings.
- [72] (First Embodiment)
- [73] Fig. 1 is a layout view of an exemplary TFT array panel for an LCD according to an embodiment of the present invention, and Fig. 2 is a sectional view of the TFT array panel shown in Fig. 1 taken along the line II-II'.
- [74] A plurality of gate lines 121 for transmitting gate signals and a plurality of storage electrode lines 131 are formed on a transparent insulating substrate 110 made of glass or transparent flexible insulator.
- [75] Each gate line 121 extends substantially in a transverse direction and a plurality of portions of each gate line 121 form a plurality of gate electrodes 124 of thin film transistor. Each gate electrode 124 may be protruded from the gate lines 121 with a various shape.
- [76] Each storage electrode line 131 extends substantially in a transverse direction. Each storage electrode line 131 may include a plurality of projections forming storage electrodes. The storage electrode lines 131 are supplied with a predetermined voltage such as the common voltage, which is applied to a common electrode of the common electrode panel (not shown) of the LCD.
- [77] The gate lines 121 and the storage lines are preferably made of low resistivity metal

including Al containing metal such as Al and Al alloy for reducing signal delay or voltage drop.

- [78] A gate insulating layer 140 preferably made of silicon nitride (SiNx) is formed on the gate lines 121 and the storage lines 131.
- [79] A plurality of semiconductor stripes 151 preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") are formed on the gate insulating layer 140. Each semiconductor stripe 151 extends substantially in a longitudinal direction and has a plurality of projections 154 branched out toward the gate electrodes 124. The width of each semiconductor stripe 151 becomes large near the gate lines 121 such that the semiconductor stripe 151 covers large areas of the gate lines 121.
- [80] A plurality of ohmic contact stripes and islands 161 and 165 preferably made of silicide or n+ hydrogenated a-Si heavily doped with n type impurity are formed on the semiconductor stripes 151. Each ohmic contact stripe 161 has a plurality of projections 163, and the projections 163 and the ohmic contact islands 165 are located in pairs on the projections 154 of the semiconductor stripes 151.
- [81] The lateral sides of the semiconductor stripes 151 and the ohmic contacts 161 and 165 are tapered, and the inclination angles thereof are preferably in a range between about 30-80 degrees.
- [82] A plurality of data lines 171 and a plurality of drain electrodes 175 separated from each other are formed on the ohmic contacts 161 and 165 and the gate insulating layer 140.
- [83] The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121 and the storage electrode lines 131.
- [84] Each drain electrodes 175 are located on the ohmic contacts 165, and it is separated from the data lines 171. The drain electrodes 175 are disposed opposite the portion of the data lines 171 with respect to a gate electrode 124, and overlap the storage electrode lines 131.
- [85] The data lines 171 include a plurality of projections such that the projections forms a source electrode 173 disposed opposite the drain electrode 175. Each set of a gate electrode 124, a source electrode 173, and a drain electrode 175 along with a projection 154 of a semiconductor stripe 151 form a TFT having a channel formed in the semiconductor projection 154 disposed between the source electrode 173 and the drain electrode 175.
- [86] The ohmic contacts 161 and 165 are interposed only between the underlying semiconductor stripes 151 and the overlying data lines 171 and the overlying drain electrodes 175 thereon and reduce the contact resistance therebetween. The semiconductor stripes 151 include a plurality of exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between

the source electrodes 173 and the drain electrodes 175. Although the semiconductor stripes 151 are narrower than the data lines 171 at most places, the width of the semiconductor stripes 151 becomes large near the gate lines as described above, to smooth the profile of the surface, thereby preventing the disconnection of the data lines 171. The portion of the semiconductor stripes 151 may be expended over the storage electrode lines 131.

- [87] At this time, the data lines 171 may have an end portion having a large area for contact with another layer or an external device.
- [88] The data lines 171 and the drain electrodes 175 are also made of material such as Al and Al alloy.
- [89] A passivation layer 180 is formed on the data lines 171 and the drain electrodes 175, and exposed portions of the semiconductor stripes 151, which are not covered with the data lines 171 and the drain electrodes 175.
- [90] The passivation layer 180 is preferably made of low dielectric insulating material such as a-Si:C:O and a-Si:O:F formed by plasma enhanced chemical vapor deposition (PECVD), organic insulator made of photosensitive organic material having a good flatness characteristic or inorganic insulator such as silicon nitride and silicon oxide. The passivation layer 180 may have a double-layered structure including a lower inorganic film and an upper organic film in order to prevent the channel portions of the semiconductor stripes 151 from being in direct contact with organic material.
- [91] The passivation layer 180 has a plurality of contact holes 182 and 185 exposing the end portions of the data lines 171 and the drain electrodes 175, respectively. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 181 exposing the end portions of the gate lines 121. The contact holes 182, 184 and 185 can have various shapes such as polygon or circle. The sidewalls of the contact holes 182, 184 and 185 are inclined with an angle of about 30-85 degrees or have stepwise profiles.
- [92] A plurality of contact layers 700 are formed on the exposed portions of the data lines 171, the drain electrodes 175, and the gate lines 121 through contact holes 181, 182 and 185, respectively. The contact layers 700 prevent the Al layer of the data lines 171, the drain electrodes 175, and the gate lines 121 through contact holes 181, 182 and 185 to expose to the air, such that the portions of the data lines 171, the drain electrodes 175, and the gate lines 121 are not eroded.
- [93] The contact layers 700 are made of material having good contact characteristics with other materials, more preferably conductive material having good contact characteristics with ITO or IZO such as an oxidized conductive material including Zr, Mo, W, or Cr.
- [94] The boundary of the contact layers 700 are the same with that of the contact holes

181, 182, 185, because the contact layers 700 are only formed on the exposed portions of the data lines 171, the drain electrodes 175, and the gate lines 121 through contact holes 181, 182 and 185, respectively.

- [95] A plurality of pixel electrodes 190, and a plurality of contact assistants 82, and 81, which are preferably made of ITO or IZO, are formed on the passivation layer 180.
- [96] A plurality of pixel electrodes 190 and a plurality of contact assistants 81 and 82, which are preferably made of transparent conductive material such as ITO and IZO or reflective conductive material such as Al and Ag, are formed on the passivation layer 180.
- [97] The pixel electrodes 190 are physically and electrically connected to the drain electrodes 175 through the contact holes 185 via the contact layer 700 such that the pixel electrodes 190 receive the data voltages from the drain electrodes 175. The pixel electrodes 190 supplied with the data voltages generate electric fields in cooperation with a common electrode on the common electrode panel (not shown), which reorient LC molecules in the LC layer disposed therebetween. A storage capacitor, which is connected in parallel to the LC capacitor CLC, is provided for enhancing the voltage storing capacity. The storage capacitors are implemented by overlapping the pixel electrodes 190 with the storage electrode lines 131. The capacitances of the storage capacitors, i.e., the storage capacitances are increased by overlapping the drain electrodes 175 with the storage electrodes lines 131.
- [98] The pixel electrodes 190 overlap the gate lines 121 and the data lines 171 to increase aperture ratio by inserting the passivation layer 180 having low dielectric insulating material therebetween.
- [99] The contact assistants 81 and 82 are connected to the exposed portion of the gate lines 121 and the exposed portion of the data lines 171 through the contact holes 181 and 182 via the contact layers 700, respectively. The contact assistants 81 and 82 are not requisites but preferred to protect the end portions of the gate lines 121 and the data lines 171 and to complement the adhesiveness of the end portions and external devices.
- [100] At this time, a contact portions are the exposed portions of the gate lines 121, the data lines 171 and the drain electrodes 175 through the contact holes 181, 182 and 185, the contact layers 700 thereon, and the portion of the pixel electrodes 190, and the contact assistants 81 and 82, which are connected to the contact layers 700.
- [101] (1st Embodiment Method)
- [102] A method of manufacturing the TFT array panel shown in Figs. 1-2 according to an embodiment of the present invention will be now described in detail with reference to Figs. 3 to 7 as well as Figs. 1 and 2.
- [103] Figs. 3, 5, 7 and 9 are layout views of the TFT array panel shown in Figs. 1 and 2 in intermediate steps of a manufacturing method thereof according to an embodiment of

the present invention, Figs. 4, 6, 8 and 10 are sectional views of the TFT array panel shown in Figs. 3, 5, 7 and 9 taken along the lines IIIB-IIIB', IVB-IVB', VB-VB', and VI-VI', respectively, and Fig. 11 is a sectional view of the TFT array panel following the step shown in Fig. 10.

- [104] A conductive film is sputtered on an insulating substrate 110 such as transparent glass. The conductive film is preferably made of Al containing metal such as Al and Al alloy.
- [105] Referring to Figs. 3 and 4, the conductive film is patterned to form a plurality of gate lines 121 including a plurality of gate electrodes 124, and a plurality of storage electrode lines 131.
- [106] Referring to Figs. 5 and 6, after sequential deposition of a gate insulating layer 140, an intrinsic a-Si layer, and an extrinsic a-Si layer, the extrinsic a-Si layer and the intrinsic a-Si layer are photo-etched to form a plurality of extrinsic semiconductor stripes 164 and a plurality of intrinsic semiconductor stripes 151 including a plurality of projections 154 on the gate insulating layer 140.
- [107] Two conductive films, a lower conductive film and an upper conductive film are sputtered in sequence. The lower conductive film is preferably made of Ti, Ta, Mo, Mo alloy or Cr, and preferably has a thickness of about 500Å. It is preferable that the upper conductive film has a thickness of about 2,500Å, and the sputtering target for the upper conductive film includes pure Al or Al alloy.
- [108] Referring to Figs. 7 and 8, the upper conductive film and the lower conductive film are wet-etched and dry-etched, respectively, or both the films are wet etched to form a plurality of data lines 171 including a plurality of source electrodes 173, and a plurality of drain electrodes 175. When the lower film is made of Mo or Mo alloy, the upper and the lower layers can be etched under the same etching conditions. The data lines 171 and the drain electrodes 175 includes the upper film 171b and 175b made of pure Al or Al alloy, and the lower film 171a and 175a made of Ti, Ta, Mo, Mo alloy or Cr,
- [109] Thereafter, portions of the extrinsic semiconductor stripes 164, which are not covered with the data lines 171, and the drain electrodes 175 are removed to complete a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 and to expose portions of the intrinsic semiconductor stripes 151. Oxygen plasma treatment preferably follows thereafter in order to stabilize the exposed surfaces of the semiconductor stripes 151.
- [110] Next, a passivation layer 180 is formed by depositing silicon nitride, by PECVD of low dielectric material such as a-Si:C:O or a-Si:O:F, or by coating a photosensitive organic insulating material having a good planarization characteristic. Referring to Figs. 9 and 10, the passivation layer 180 as well as the gate insulating layer 140 is photo-etched to form a plurality of contact holes 181, 182 and 185. When forming the

passivation layer made of photosensitive organic insulating material, it is not necessary that the photoresist pattern is used as etch mask, and the passivation layer 180 is exposed and developed in photo process using a photo mask.

- [111] Next, referring to Fig. 11, the insulating substrate 110 is soaked in chemical conversion solution to form a plurality of contact layer 700 on the end portion of the gate lines 121 and the data lines 171, and the portion of the drain electrode 175, which are exposed through the contact holes 181, 182 and 185. The chemical conversion solution preferably includes metal material such as Zr, Mo, Cr, W.
- [112] After etching the passivation layer 180 to form the contact holes 181, 182 and 185, an aluminum oxidation layers are formed on the exposed portion of the gate lines 121 and the data lines 171, and the drain electrode 175 by being exposed in the air. The aluminum oxidation layers deteriorate the electric contact properties with other subsequent layer.
- [113] Next, when the insulating substrate 110 is soaked in chemical conversion solution, Al metal of aluminum oxide layers substitutes for metal material such as W, Zr, Mo, Cr in the chemical conversion solution. Accordingly, the contact layers 700 including as W, Zr, Mo, or Cr are formed on the end portion of the gate lines 121 and the data lines 171, and the portion of the drain electrode 175, and the aluminum oxide layers are removed.
- [114] The contact layers 700 is a conductive oxide layer, and the chief ingredient of the contact layers 700 changes depend on the metal element of the chemical conversion solution such as zirconium oxide, tungsten oxide or chromium oxide. For an example, the chemical conversion solution including Na_2ZrO_4 , NaWO_3 , and F- is used to form the contact layers 700 made of zirconium oxide.
- [115] Because the contact layers 700 are formed after the contact holes 181, 182, 185, the contact layers 700 have almost the same planar shapes as the contact holes 181, 182, 185.
- [116] Finally, as shown in Figs. 1 and 2, an ITO or IZO layer with a thickness in a range between about 500Å and about 1,500Å is sputtered and photo-etched to form a plurality of pixel electrodes 190, and a plurality of contact assistants 81 and 82. At this time, the pixel electrodes 190, and the plurality of contact assistants 81 and 82 are respectively connected to the drain electrode 175, and the end portions of the gate lines 121 and the data lines 171 via the contact layers 700.
- [117] In the TFT array panel according to an embodiment of the present invention, when the gate lines 121 and the data lines 171 Al or Al alloy with low resistivity are formed, the process inserting different material to improve contact characteristics can be omitted by forming the contact layers 700. Accordingly, the manufacturing process of the TFT array panel can be simplified, the TFT array panel with large scale and high

fineness can easily manufactured.

[118] Furthermore, it is not necessary that the signal lines including aluminum are formed of multi-layered structure, and therefore the problems such as bending of the panel along the longitude direction can be minimized in sputtering process.

[119] Also, since there is no undercut at the contact holes 181, 182 and 185 and thus the contact inferiority in the contact portions are prevented. Accordingly, the reliability of the contact portions can be improved and the contact resistance of the contact portions can be minimized.

[120] At this time, the thickness of the zirconium oxide layer is less than 0.2 μm , and the contact layers have sheet resistance of less than 35,000ohm/cm²

[121] (2nd Embodiment Structure)

[122] A TFT array panel for an LCD according to another embodiment of the present invention will be described in detail with reference to Figs. 12 and 13.

[123] Fig. 12 is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention, and Fig. 13 is sectional view of the TFT array panel shown in Fig. 12 taken along the line IX-IX.

[124] As shown in Figs. 12 and 13, a layered structure of a TFT array panel of an LCD according to this embodiment is almost the same as that shown in Figs. 1 and 2. That is, a plurality of gate lines 121 including a plurality of gate electrodes 124, and a plurality of storage electrode lines 131 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of contact holes 181, 182 and 185 are provided at the passivation layer 180 and/or the gate insulating layer 140, and a plurality of pixel electrodes 190 and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180.

[125] Different from the TFT array panel shown in Figs. 1 and 2, the semiconductor stripes 151 have almost the same planar shapes as the data lines 171 and the drain electrodes 175 as well as the underlying ohmic contacts 161 and 165, except for the projections 154 where TFTs are provided. That is, the semiconductor stripes 151 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175, such as portions located between the source electrodes 173 and the drain electrodes 175.

[126] (2nd Embodiment Method)

[127] Now, a method of manufacturing the TFT array panel shown in Figs. 12 and 13

according to an embodiment of the present invention will be described in detail with reference to Figs. 14-15 as well as Figs. 12 and 13.

- [128] Figs. 14, 18, and 20 are layout views of the TFT array panel shown in Figs. 12 and 13 in intermediate steps of a manufacturing method thereof according to another embodiment of the present invention; Fig. 15 is sectional view of the TFT array panel shown in Fig. 14 taken along the lines XB-XB'; Fig. 16 is a sectional view of the TFT array panel following the step shown in Fig. 15; Fig. 17 is a sectional view of the TFT array panel following the step shown in Fig. 16; Fig. 19 is sectional view of the TFT array panel shown in Fig. 18 taken along the lines XIII B-XIII B'; Fig. 21 is sectional view of the TFT array panel shown in Fig. 20 taken along the lines XIV B-XIV B'; and Fig. 22 is a sectional view of the TFT array panel following the step shown in Fig. 21.
- [129] Referring to Figs. 14 and 15, a plurality of gate lines 121 including a plurality of gate electrodes 124, and a plurality of storage electrode lines 131 are formed on a substrate 110 by photo etching.
- [130] As shown in Fig. 16, a gate insulating layer 140, an intrinsic a-Si layer 150, and an extrinsic a-Si layer 160 are sequentially deposited by CVD such that the layers 140, 150 and 160. A conductive layer 170 including a lower film 170a made of Al or Al alloy and an upper film 170b made of metal such as Cr, Ti, Ta, Mo and their alloy is deposited by sputtering, and a photoresist film with the thickness of about 1-2 microns is coated on the conductive layer 170.
- [131] The photoresist film is exposed to light through an exposure mask (not shown); and developed such that the developed photoresist has a position dependent thickness.
- [132] The photoresist shown in Figs. 16 includes a plurality of first to third portions with decreased thickness. The first portions located on wire areas A and the second portions located on channel areas B are indicated by reference numerals 52 and 54, respectively, and no reference numeral is assigned to the third portions located on remaining areas C since they have substantially zero thickness to expose underlying portions of the conductive layer 170. The thickness ratio of the second portions 54 to the first portions 52 is adjusted depending upon the process conditions in the subsequent process steps.
- [133] The position-dependent thickness of the photoresist is obtained by several techniques, for example, by providing translucent areas on the exposure mask as well as transparent areas and light blocking opaque areas. The translucent areas may have a slit pattern, a lattice pattern, a thin film(s) with intermediate transmittance or intermediate thickness. When using a slit pattern, it is preferable that the width of the slits or the distance between the slits is smaller than the resolution of a light exposer used for the photolithography. Another example is to use reflowable photoresist. In detail, once a photoresist pattern made of a reflowable material is formed by using a

normal exposure mask only with transparent areas and opaque areas, it is subject to reflow process to flow onto areas without the photoresist, thereby forming thin portions.

- [134] The different thickness of the photoresist 52 and 54 enables to selectively etch the underlying layers when using suitable process conditions. Therefore, a plurality of data lines 171 including a plurality of source electrodes 173, and a plurality of drain electrodes 175, as well as a plurality of ohmic contact stripes 161 including a plurality of projections 163, a plurality of ohmic contact islands 165 and a plurality of semi-conductor stripes 151 including a plurality of projections 154 are obtained as shown in Figs. 18 and 19 by a series of etching steps.
- [135] For descriptive purpose, portions of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 on the wire areas A are called first portions, portions of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 on the channel areas B are called second portions, and portions of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 on the remaining areas C are called third portions.
- [136] An exemplary sequence of forming such a structure is as follows:
- [137] (1) Removal of third portions of the conductive layer 170, the extrinsic a-Si layer 160 and the intrinsic a-Si layer 150 on the wire areas A;
- [138] (2) Removal of the second portions 54 of the photoresist;
- [139] (3) Removal of the second portions of the conductive layer 170 and the extrinsic a-Si layer 160 on the channel areas B; and
- [140] (4) Removal of the first portions 52 of the photoresist.
- [141] Another exemplary sequence is as follows:
- [142] (1) Removal of the third portions of the conductive layer 170;
- [143] (2) Removal of the second portions 54 of the photoresist;
- [144] (3) Removal of the third portions of the extrinsic a-Si layer 160 and the intrinsic a-Si layer 150;
- [145] (4) Removal of the second portions of the conductive layer 170;
- [146] (5) Removal of the first portions 52 of the photoresist; and
- [147] (6) Removal of the second portions of the extrinsic a-Si layer 160.
- [148] The first example is described in detail.
- [149] Referring to Fig. 17, the exposed third portions of the conductive layer 170 on the remaining areas C are removed by wet etching or dry etching to expose the underlying third portions of the extrinsic a-Si layer 160.
- [150] Reference numeral 174 indicates portions of the conductive layer 170 including the data lines 171 and the drain electrode 175 connected to each other and lower, and upper films thereof are indicated by reference numerals 174a and 174b, respectively.

The dry etching may etch out the top portions of the photoresist 52 and 54.

[151] Next, the third portions of the extrinsic a-Si layer 160 on the areas C and of the intrinsic a-Si layer 150 are removed preferably by dry etching and the second portions 54 of the photoresist are removed to expose the second portions of the conductors 174. The removal of the second portions 54 of the photoresist are performed either simultaneously with or independent from the removal of the third portions of the extrinsic a-Si layer 160 and of the intrinsic a-Si layer 150. Residue of the second portions 54 of the photoresist remained on the channel areas B is removed by ashing.

[152] The semiconductor stripes 151 are completed in this step, and reference numeral 164 indicates portions of the extrinsic a-Si layer 160 including the ohmic contact stripes and islands 161 and 165 connected to each other, which are called "extrinsic semiconductor stripes."

[153] The lower film 170a of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 are dry-etched in sequence to simplify the manufacturing process. In this case, the dry etching of the three film and layers 170a, 160 and 150 may be performed in-situ in a single etching chamber.

[154] Referring to Figs. 18 and 19, the second portions of the conductors 174 and the extrinsic a-Si stripes 164 on the channel areas B as well as the first portion 52 of the photoresist are removed.

[155] In case that the exposed portions of the extrinsic semiconductor stripes 164 is removed using the data lines 171 and the drain electrodes 175 as an etch mask after removing the photoresist film.

[156] At this time, top portions of the projections 154 of the intrinsic semiconductor stripes 151 on the channel areas B may be removed to cause thickness reduction.

[157] In this way, each conductor 174 is divided into a data line 171 and a plurality of drain electrodes 175 to be completed, and each extrinsic semiconductor stripe 164 is divided into an ohmic contact stripe 161 and a plurality of ohmic contact islands 165 to be completed.

[158] Referring to Figs. 20 and 21, a passivation layer 180 is formed by the CVD of a silicon nitride film, by the coating of an acrylic organic insulating film, or by the PECVD of low dielectric insulating material such as a-Si:C:O and a-Si:O:F. Thereafter, the passivation layer 180 and the gate insulating layer 140 are photo-etched to form a plurality of contact holes 181, 182 and 185.

[159] Referring to Fig 22., the insulating substrate 110 is soaked in chemical conversion solution with the same method as that in previous embodiment to form a plurality of contact layer 700 on the end portion of the gate lines 121 and the data lines 171, and the portion of the drain electrode 175, which are exposed through the contact holes 181, 182 and 185.

- [160] Finally, as shown in Figs. 12 and 13, a plurality of pixel electrodes 190 and a plurality of contact assistants 81 and 82 are formed on the passivation layer 180 by sputtering and photo-etching an ITO or IZO layer.
- [161] When the passivation layer 180 includes the organic material having lower dielectric constant, the pixel electrodes 190 are expanded over the data lines 171 to increase the aperture ratio.
- [162] At this time, the storage electrode lines 131 may have a contact portion to receive signals such as common voltage from the external device. The contact portion includes a contact hole to expose the portion of the storage electrode lines 131, a contact assistant connected to the storage electrode lines 131, and a contact layer, which is made of conductive oxide layer and is located between the contact assistant and the portion of the storage electrode lines 131.
- [163] On the other hand, the THT array panel may include a plurality of gate driving circuit to apply scanning signals to the gate lines 121. At this time, the gate driving circuits may be formed through the same manufacturing method as that of thin film transistors of pixel areas, and a layered structure of the gate driving circuits is almost the same as that of thin film transistor of pixel.
- [164] A plurality of thin film transistor consisting of the gate driving circuits are electrically connected to each other via a plurality of signal lines, and the signal lines include the conductive layers made of a layered structure of the gate lines 121 or the data lines 171. At this time, the signal lines may also have a contact portion to connect to the conductive layers to each other, which are located at the different layer. The contact portion includes a contact hole to expose the portion of the conductive layer of the signal lines, a contact assistant connected to the signal lines, and a contact layer, which is made of conductive oxide layer and is located between the contact assistant and the portion of the signal lines.
- [165] (3rd Embodiment structure)
- [166] Different from the above-described TFT array panels, a TFT array panel according to this embodiment may further include a plurality of color filters.
- [167] A TFT array panel for an LCD according to this embodiment of the present invention will be described in detail with reference to Figs. 23 and 24.
- [168] Fig. 23 is a layout view of an exemplary TFT array panel for an LCD according to another embodiment of the present invention; and Fig. 24 is sectional view of the TFT array panel shown in Fig. 23 taken along the line XVII-XVII'.
- [169] As shown in Figs. 23 and 24, a layered structure of a TFT array panel of an LCD according to this embodiment is almost the same as that shown in Figs. 1 and 2.
- [170] Different from the previous embodiments, a plurality of red, green and blue color filter stripes 230R, 230G and 230B are formed on the passivation layer 180 covering

the data lines 171, and the drain electrodes 175. Each of the color filter stripes 230R, 230G and 230B is disposed substantially between adjacent two of the data lines 171 and extends in a longitudinal direction. The color filter stripes 230R, 230G and 230B may be divided into a plurality of color filters disposed in respective pixel areas defined by the gate lines 121 and the data lines 171. Although edges of adjacent color filter stripes 230R, 230G and 230B exactly match with each other, the color filter stripes 230R, 230G and 230B overlap each other to block the light leakage between the pixel areas. The three color filters may overlap each other between the pixel areas on the data lines 171.

[171] The color filter stripes 230R, 230G and 230B are not disposed on a peripheral area which is provided with the contact portions of the gate lines 121 and the data lines 171.

[172] An interlayer insulating layer 801 is formed on the adjacent color filter stripes 230R, 230G and 230B. The interlayer insulating layer 801 prevents the resin of the color filter stripes 230R, 230G and 230B from penetrating into the pixel electrode 190, may be omitted.

[173] In this embodiment, a black matrix of a common electrode panel opposite the TFT array panel can be only formed on the positions correspond to the thin film transistors, such that the aperture ratio of pixels is increased.

[174] (3rd Embodiment Method)

[175] Now, a method of manufacturing the TFT array panel shown in Figs. 23 and 24 according to an embodiment of the present invention will be described in detail with reference to Figs. 25-29 as well as Figs. 23 and 24.

[176] Figs. 25 and 27 are layout views of the TFT array panel shown in Figs. 23 and 24 in intermediate steps of a manufacturing method thereof according to another embodiment of the present invention; Fig. 26 is sectional view of the TFT array panel shown in Fig. 25 taken along the lines XVIII B-XVIII B'; Fig. 28 is sectional view of the TFT array panel shown in Fig. 27 taken along the lines XIX B-XIX B'; and Fig. 29 is a sectional view of the TFT array panel following the step shown in Fig. 28.

[177] Referring to Figs. 3 to 8, a plurality of gate lines 121, a plurality of storage electrode lines 131, an gate insulating layer 140, a plurality of semiconductor stripes 151, a plurality of ohmic contact stripes and islands 161 and 165 a plurality of data lines 171 including a plurality of source electrodes 173, and a plurality of drain electrodes 175 are formed on an insulating substrate 110.

[178] Referring to Figs. 25 to 26, after depositing a passivation layer 180 made on inorganic material such as silicon nitride or silicon oxide, three photosensitive film are sequentially coated on the upper surface of the insulating substrate 110. The three negative photosensitive films are a water-insoluble dispersion solution respectively containing a photopolymerizable photosensitive composition including photopoly-

merization initiators, monomers, binders, etc., and one of red, green and blue pigments. Thereafter, the photosensitive films are respectively exposed to light through a mask for color filter to form a plurality of color filter stripes 230R, 230G and 230B. Each color filter stripes 230R, 230G and 230B have a plurality of contact holes 235 exposing the portion of the drain electrodes 175

- [179] Referring to Figs. 27 and 28, a interlayer insulating layer 801 is formed by the coating of an organic insulating film having low dielectric less than 4.0, or by the PECVD of low dielectric insulating material such as a-Si:C:O and a-Si:O:F. Thereafter, the interlayer insulating layer 801 is photo-etched to form a plurality of contact holes 182 and 185 respectively exposing the portion of the drain electrode 175 inside the contact hole 235 and the end portion of the data lines 171.
- [180] Next, referring to Fig. 29, the insulating substrate 110 is soaked in chemical conversion solution to form a plurality of contact layers 700 on the end portion of the data lines 171 and the portion of the drain electrode 175, like as previous embodiments.
- [181] Finally, as shown in Figs. 23 and 24, an ITO or IZO layer is sputtered and photo-etched to form a plurality of pixel electrodes 190, and a plurality of contact assistants 82.
- [182] In the TFT array panel according to an embodiment of the present invention, the signal lines made of Al or Al alloy with low resistivity are easily applicable by forming the contact layers, such that the TFT array panel with large scale and high fineness is provided.
- [183] While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

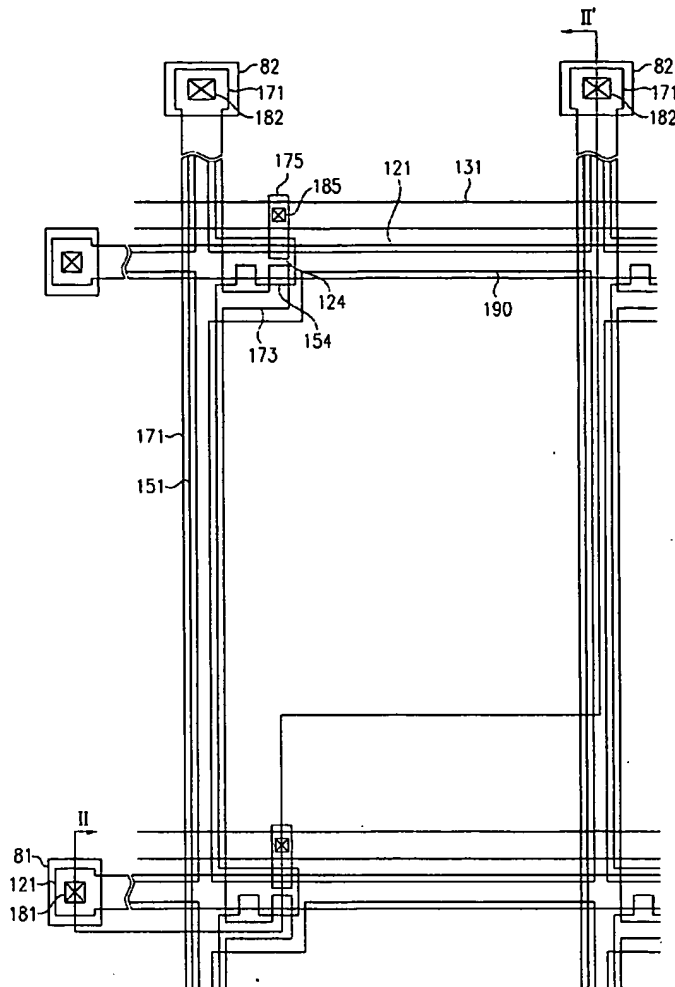
Claims

- [1] A method of manufacturing a contact portion, the method comprising:
forming a first signal line on a substrate;
forming an insulating layer covering the first signal line and having a contact hole exposing the first signal line;
forming a contact layer on the exposed surface of the first signal through the contact hole; and
forming a second signal line connected to the first signal line via the contact layer,
wherein the first signal line is made of Al or Al alloy, and the second signal line is made of ITO or IZO.
- [2] The method of claim 1, wherein the substrate is soaked in chemical conversion solution including a conductive material to form the contact layer.
- [3] The method of claim 2, wherein chemical conversion solution include at least one of W, Zr, Mo, and Cr.
- [4] A method of manufacturing a thin film transistor array panel, the method comprising:
forming a gate line on a substrate;
forming a gate insulating layer;
forming a semiconductor layer;
forming an ohmic contact layer;
forming a data line and a drain electrode;
forming a passivation layer having a first contact hole exposing the portion of the drain electrode; and
forming a first contact layer on the exposed surface of the drain electrode through the first contact hole.
- [5] The method of claim 4, wherein the substrate is soaked in chemical conversion solution including a conductive material to form the contact layer.
- [6] The method of claim 5, wherein chemical conversion solution include at least one of W, Zr, Mo, and Cr.
- [7] The method of claim 4, wherein a second contact hole exposing the end portion of the gate line or the data line is formed in the step of forming the passivation layer.
- [8] The method of claim 7, wherein a second contact layer is formed on the exposed surface of the gate line or the data line through the second contact hole in the step of forming the first contact layer.
- [9] The method of claim 4, further comprising a step of forming a storage electrode

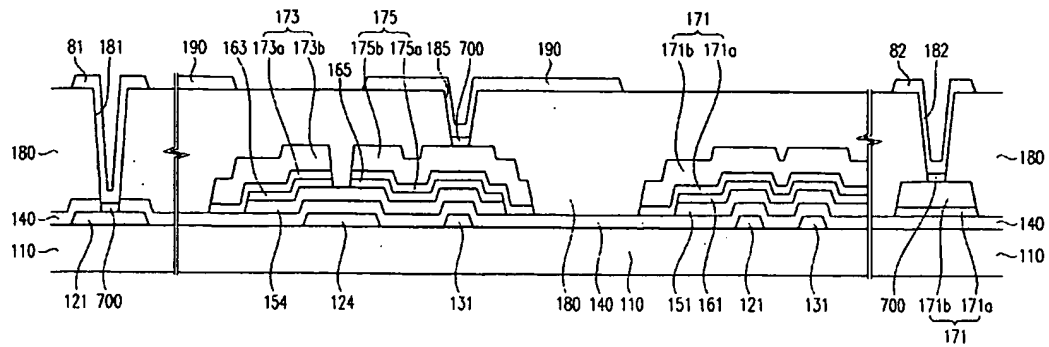
- line with the same layer as the gate line.
- [10] The method of claim 8, wherein a second contact hole exposing the end portion of the storage electrode line is formed in the step of forming the passivation layer.
- [11] The method of claim 9, wherein a second contact layer is formed on the exposed surface of the storage electrode line through the second contact hole in the step of forming the first contact layer.
- [12] A contact portion comprising:
a substrate;
a first signal line formed on a substrate;
an insulating layer covering the first signal line and having a contact hole exposing the first signal line;
a contact layer on the exposed surface of the first signal through the contact hole;
and
a second signal line formed on the insulating layer and connected to the first signal line via the contact layer,
wherein the first signal line is made of Al or Al alloy, and the second signal line is made of ITO or IZO.
- [13] The contact portion of claim 12, wherein the contact layer include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr.
- [14] The contact portion of claim 12, further comprising a lower layer formed under the first signal line.
- [15] The contact portion of claim 14, wherein the lower layer is a conductive layer including at least one of Cr, Ti, Mo, and MoW alloy.
- [16] A thin film transistor array panel comprising:
a substrate;
a gate line formed on a substrate;
a gate insulating layer covering the gate line;
a semiconductor layer formed on the gate insulating layer;
a data line intersecting the gate line and having a source electrode overlapping the portion of the semiconductor layer;
a drain electrode overlapping the portion of the semiconductor layer;
a passivation layer covering the data line and the drain electrode, and having a first contact hole exposing the portion of the drain electrode;
a first contact layer formed on the exposed surface of the drain electrode through the first contact hole, and made of a conductive oxide layer; and
a pixel electrode formed on the passivation layer and connected to the drain electrode via the first contact layer.

- [17] The panel of claim 16, further comprising a color filter formed on the data line and the drain electrode.
- [18] The panel of claim 16, further comprising a storage electrode line formed with the same layer as the gate line.
- [19] The panel of claim 18, wherein the storage electrode line includes Al and Al alloy.
- [20] The panel of claim 18, wherein the passivation layer and the gate insulating layer have a second contact hole exposing the portion of the storage electrode line, further comprising a second contact layer formed on the exposed portion on the storage electrode line through the contact hole; and a contact assistant connected to the exposed portion of the storage electrode line via the second contact layer.
- [21] The panel of claim 20, wherein the second contact layer include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr.
- [22] The panel of claim 16, wherein the passivation layer or the gate insulating layer have a third contact hole exposing the portion of the gate line or the data line, further comprising a third contact layer formed on the exposed portion on the gate line or the data line through the third contact hole; and a contact assistant connected to the exposed portion of the gate line or the data line via the third contact layer.
- [23] The panel of claim 22, wherein the third contact layer include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr.
- [24] The panel of claim 16, further comprising an ohmic contact layer formed between the data line and the drain electrode, and the semiconductor layer.
- [25] The panel of claim 24, wherein the ohmic contact layer has the same planar shape as the data line and the drain electrode, and the semiconductor layer has the planar shape as the data line and the drain electrode except for the channel portion between the drain electrode and the source electrode.
- [26] The panel of claim 16, wherein the first contact layer include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr.
- [27] The panel of claim 16, wherein the gate line includes a conductive layer made of Al or Al alloy.
- [28] The panel of claim 16, wherein the data line includes a first conductive layer made of Al or Al alloy.
- [29] The panel of claim 28, wherein the data line further comprise a second conductive layer formed under the first conductive layer.
- [30] The panel of claim 29, wherein the second conductive layer is made of a conductive layer including at least one of Cr, Ti, Mo, and MoW alloy.

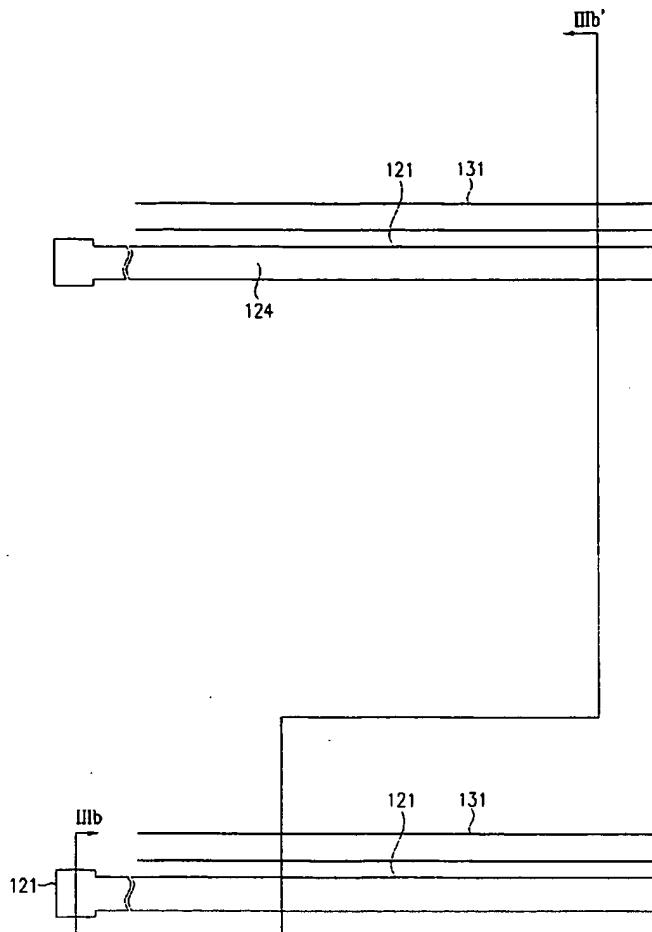
[Fig. 1]



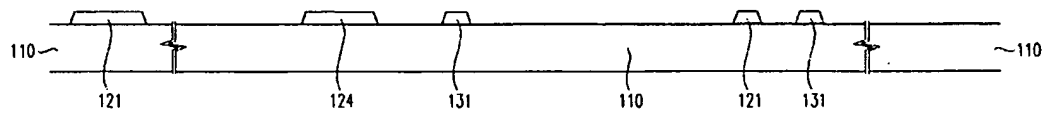
[Fig. 2]



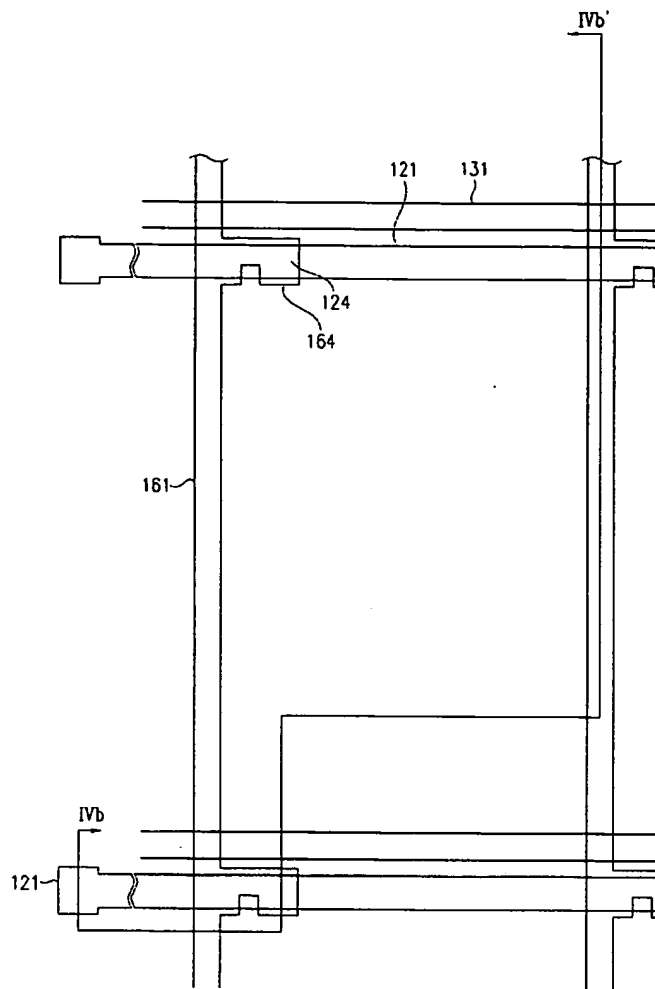
[Fig. 3]



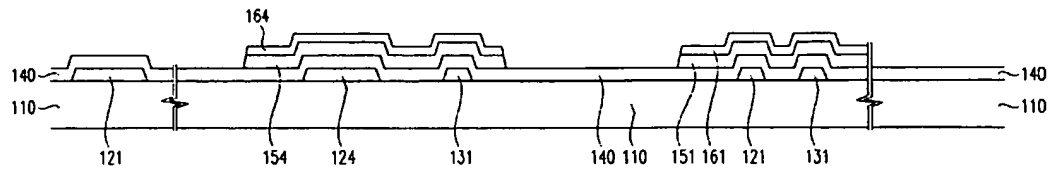
[Fig. 4]



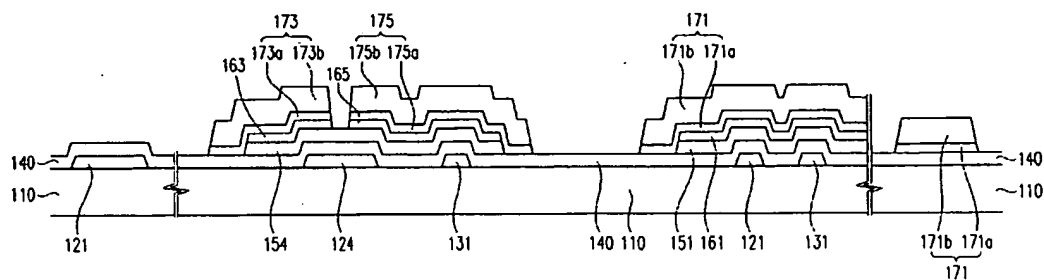
[Fig. 5]



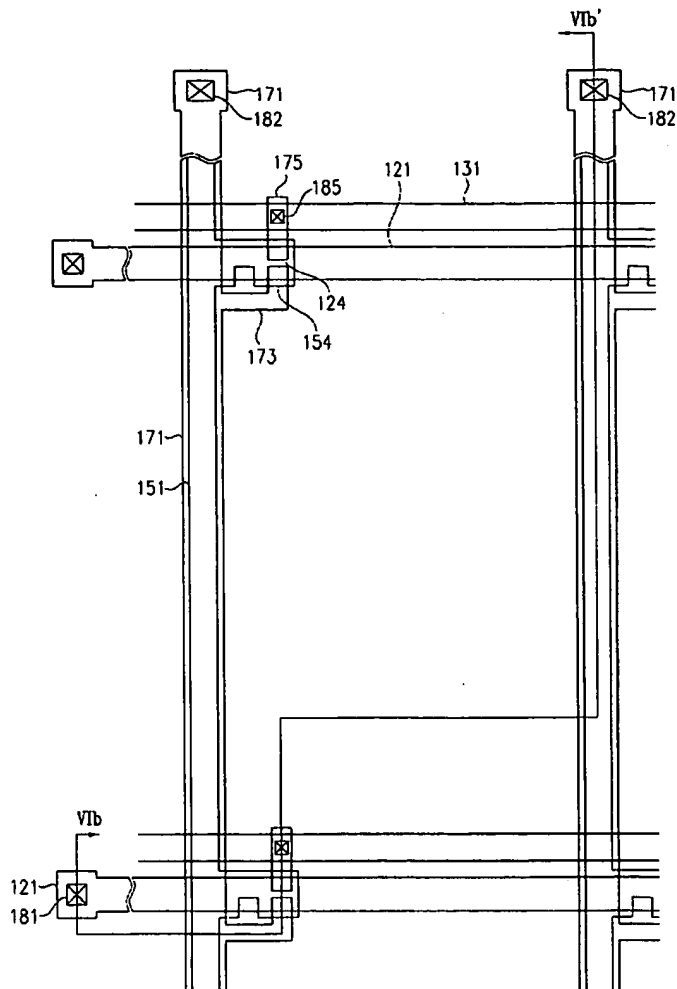
[Fig. 6]



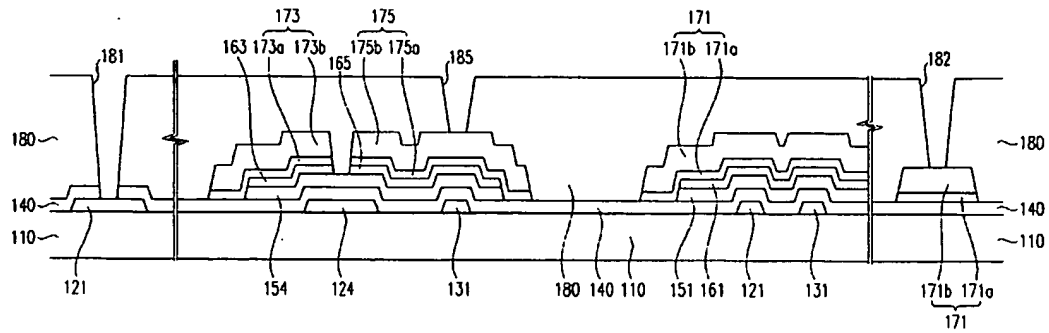
[Fig. 8]



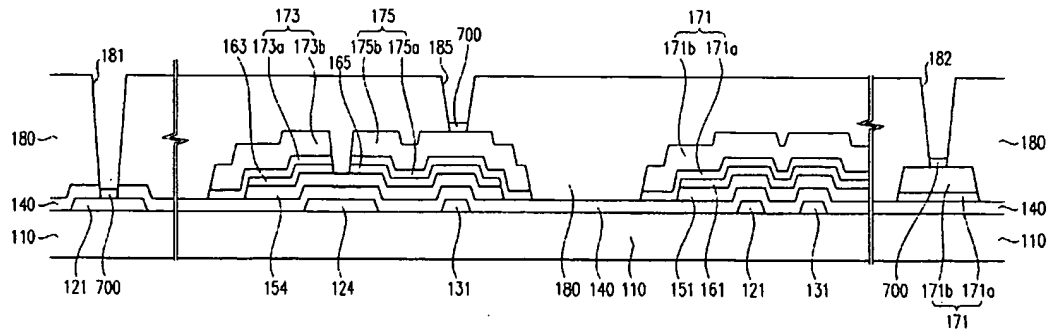
[Fig. 9]



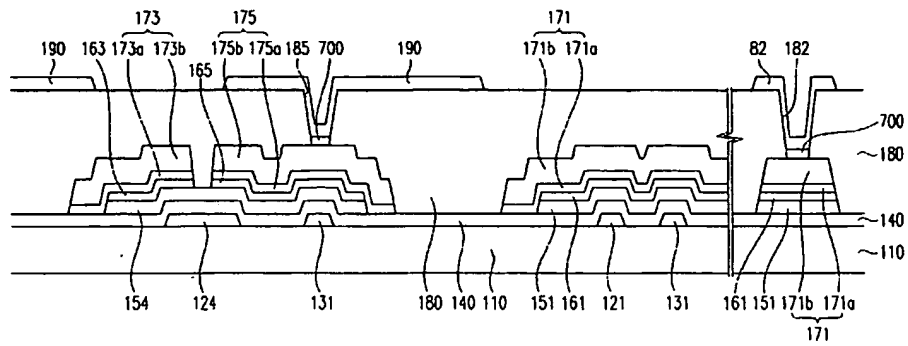
[Fig. 10]



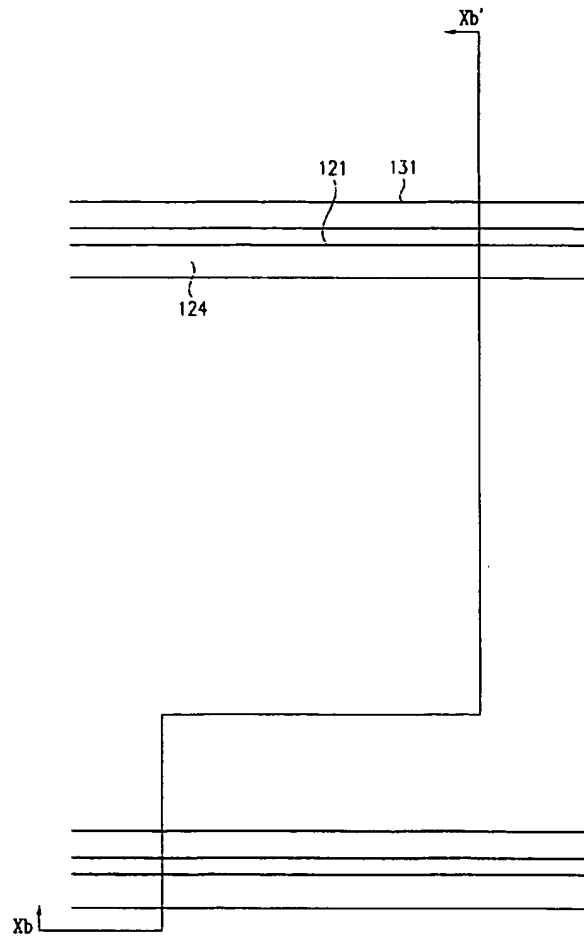
[Fig. 11]



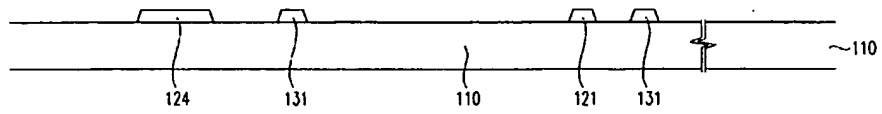
[Fig. 13]



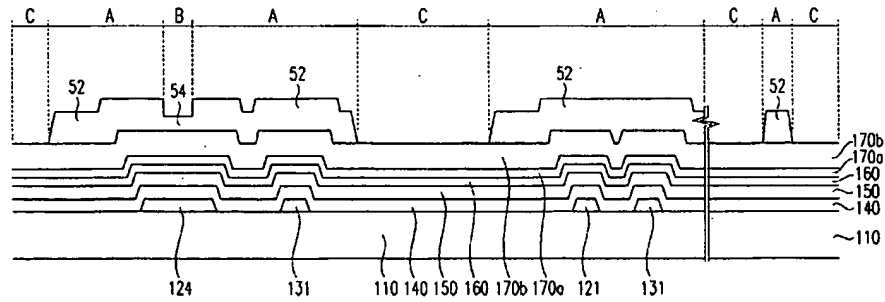
[Fig. 14]



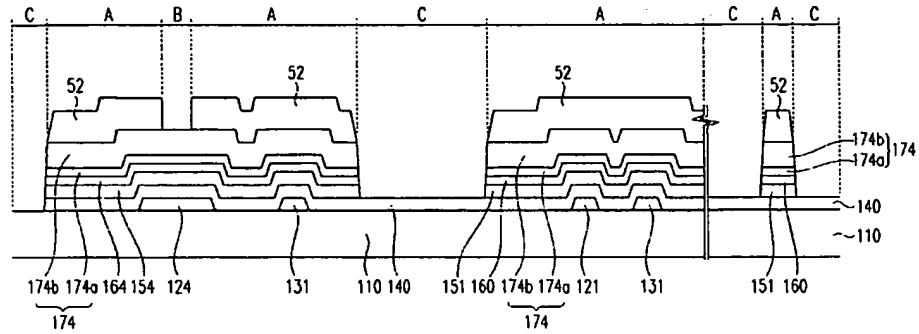
[Fig. 15]



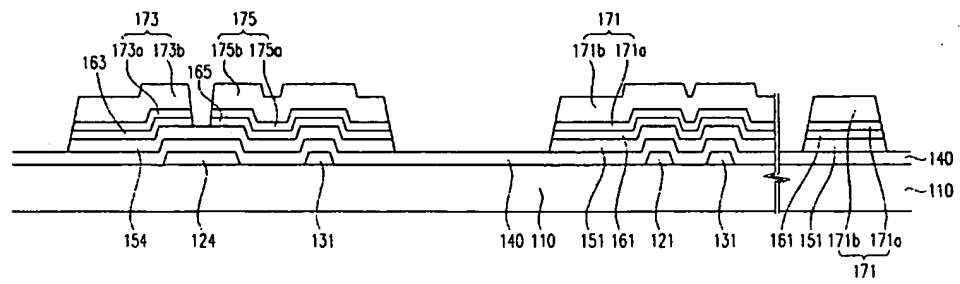
[Fig. 16]



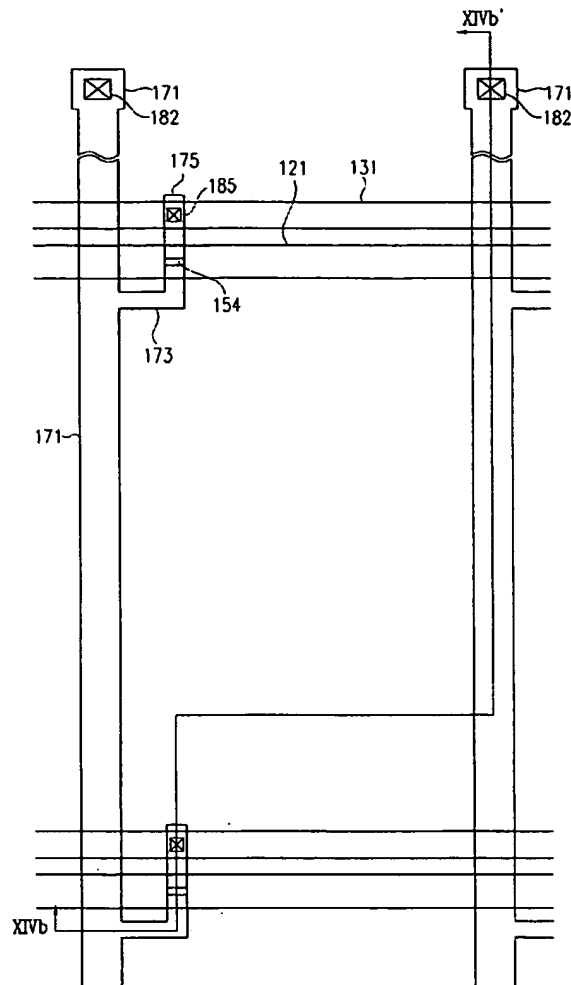
[Fig. 17]



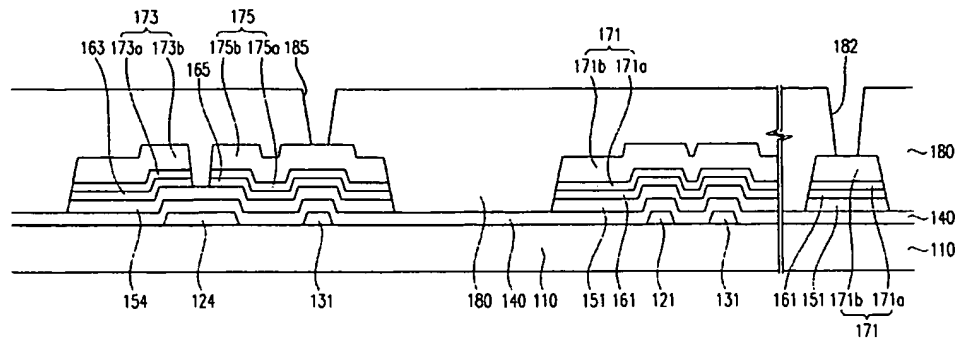
[Fig. 19]



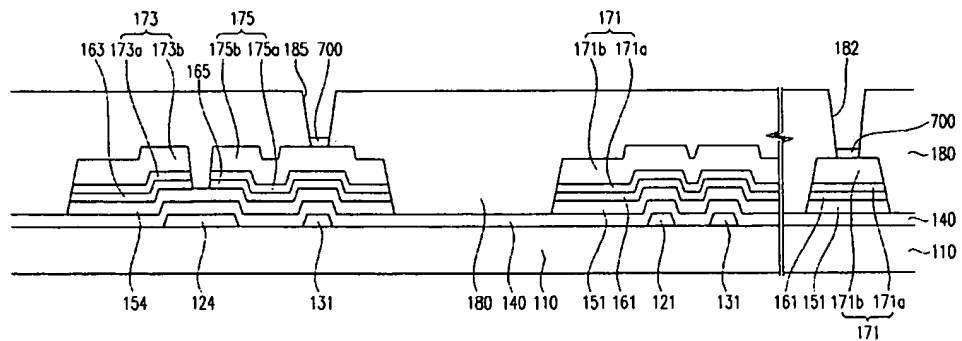
[Fig. 20]



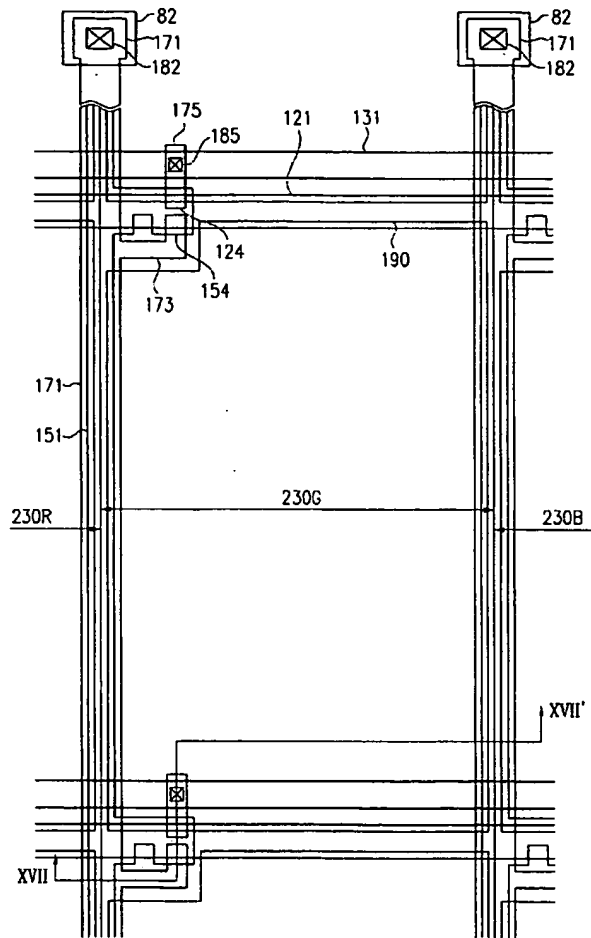
[Fig. 21]



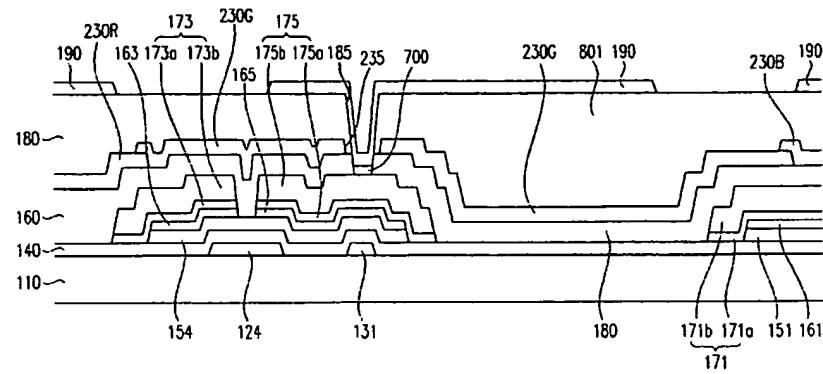
[Fig. 22]



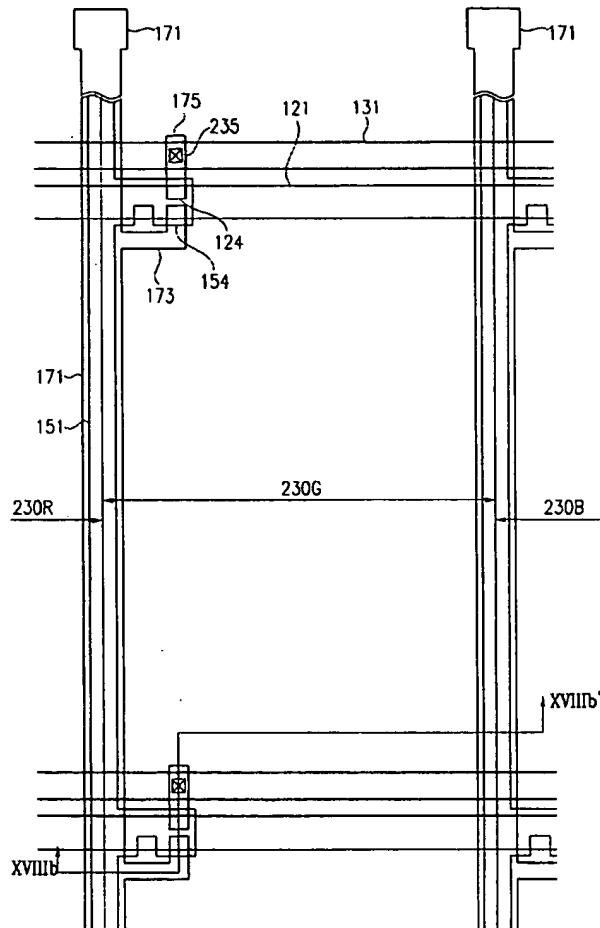
[Fig. 23]



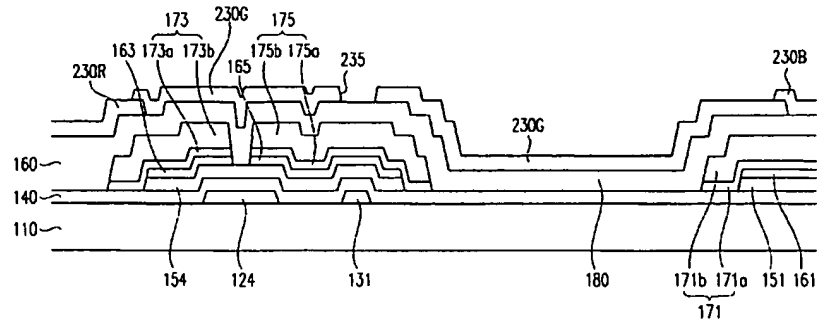
[Fig. 24]



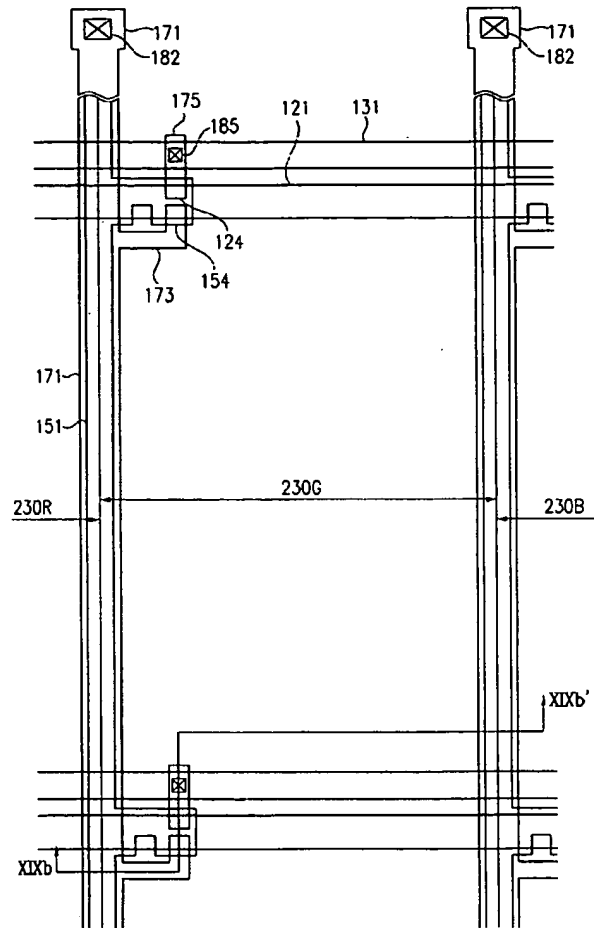
[Fig. 25]



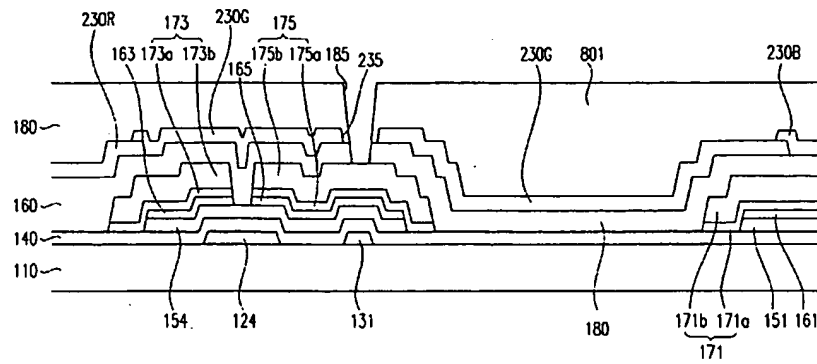
[Fig. 26]



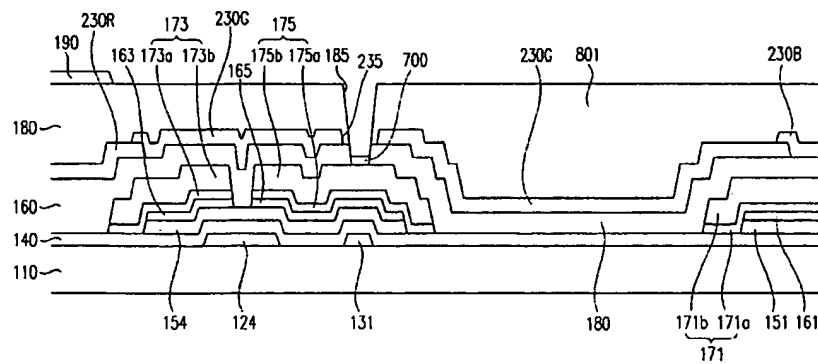
[Fig. 27]



[Fig. 28]



[Fig. 29]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 2005/000392

A. CLASSIFICATION OF SUBJECT MATTER IPC ⁷ : H01L 21/768, H01L 23/532, G02F 1/1362 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC ⁷ : H01L, G02F Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) Epodoc, WPI, PAJ, TXT		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 1041622 A1 (SEMICONDUCTOR ENERGY) 4 October 2000 (04.10.2000) <i>paragraphs 0013-0018; figure 1.</i>	1-30
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A	US 6524876 B1 (SAMSUNG) 25 February 2003 (25.02.2003) <i>figure 10 and the associated description.</i>	1-30
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A	US 20030058379 A1 (LEE) 27 March 2003 (27.03.2003) <i>paragraphs 0015-0026; figures 1A-1D.</i>	1-30

<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 14 June 2005 (14.06.2005)		Date of mailing of the international search report 27 June 2005 (27.06.2005)
Name and mailing address of the ISA/ AT Austrian Patent Office Dresdner Straße 87, A-1200 Vienna Facsimile No. +43 / 1 / 534 24 / 535		Authorized officer HARASEK S. Telephone No. +43 / 1 / 534 24 / 574

INTERNATIONAL SEARCH REPORT

information on patent family members

International application No.

PCT/KR 2005/000392

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